

Fig. 1A

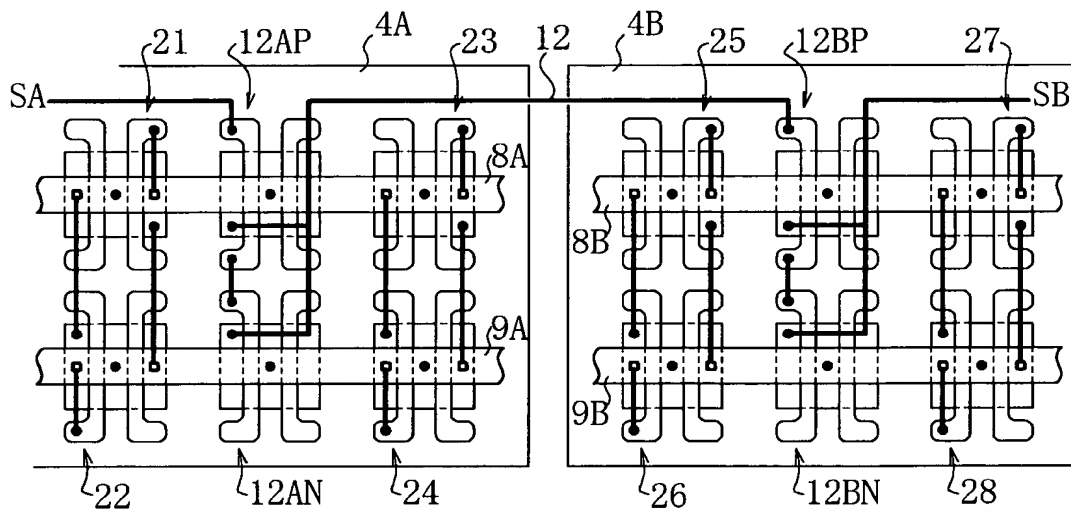


Fig. 1B

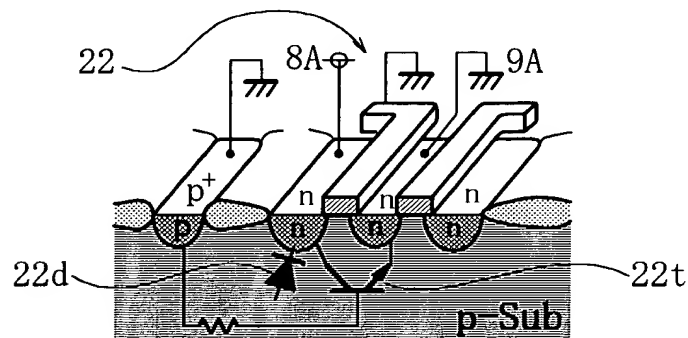


Fig. 1C

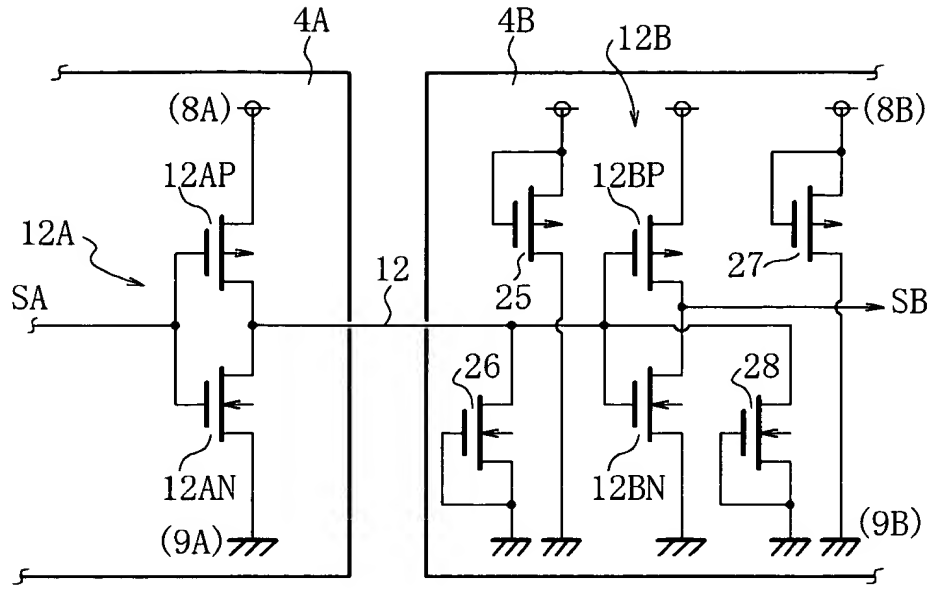


Fig. 2A

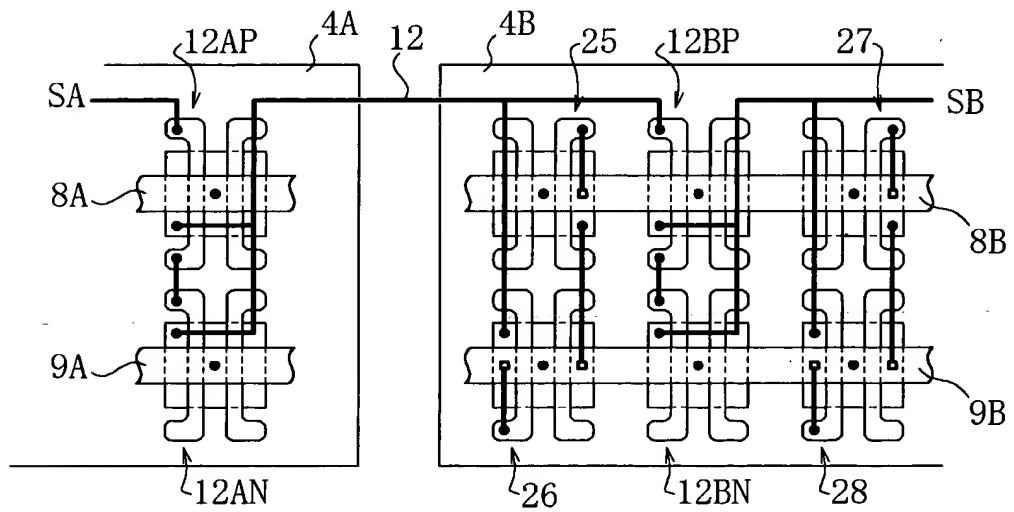


Fig. 2B

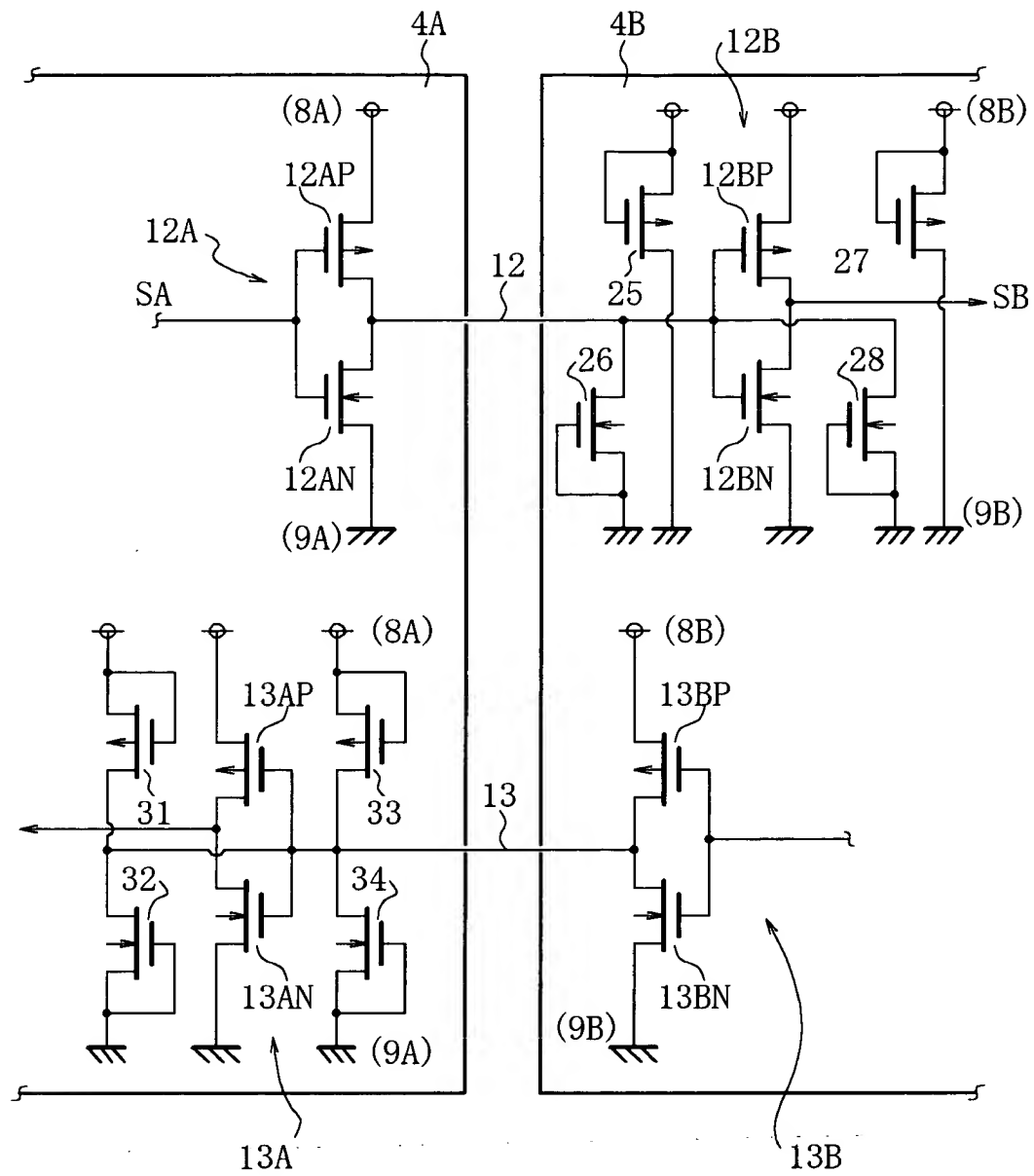


Fig. 3

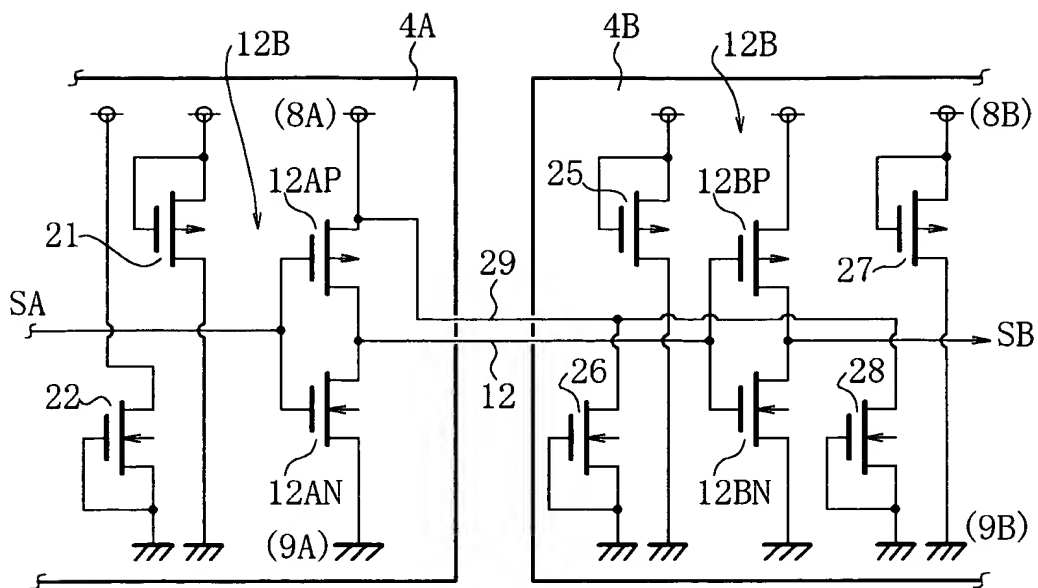


Figure 1 is a plan view of a semiconductor device. It shows two semiconductor chips, 8A and 8B, mounted on a substrate 12. Chip 8A is on the left, and chip 8B is on the right. They are connected by a central bus 29. Various pads and connections are labeled: 21, 12AP, 4A, 29, 4B, 25, 12BP, 27, SA, SB, 8A, 8B, 9A, 9B, 22, 12AN, 26, 12BN, 28.

Fig. 5B

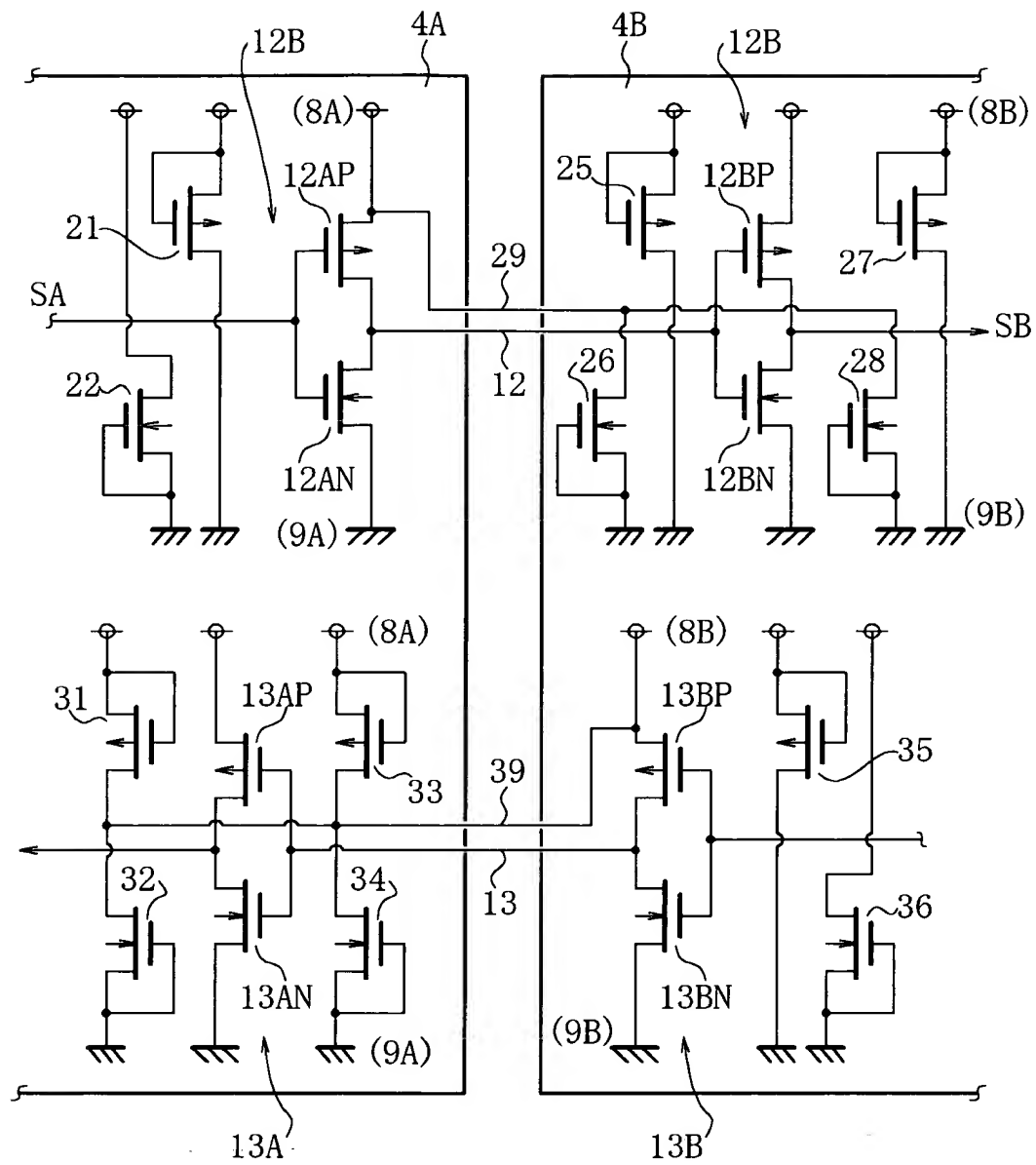


Fig. 6

005240" 4952960

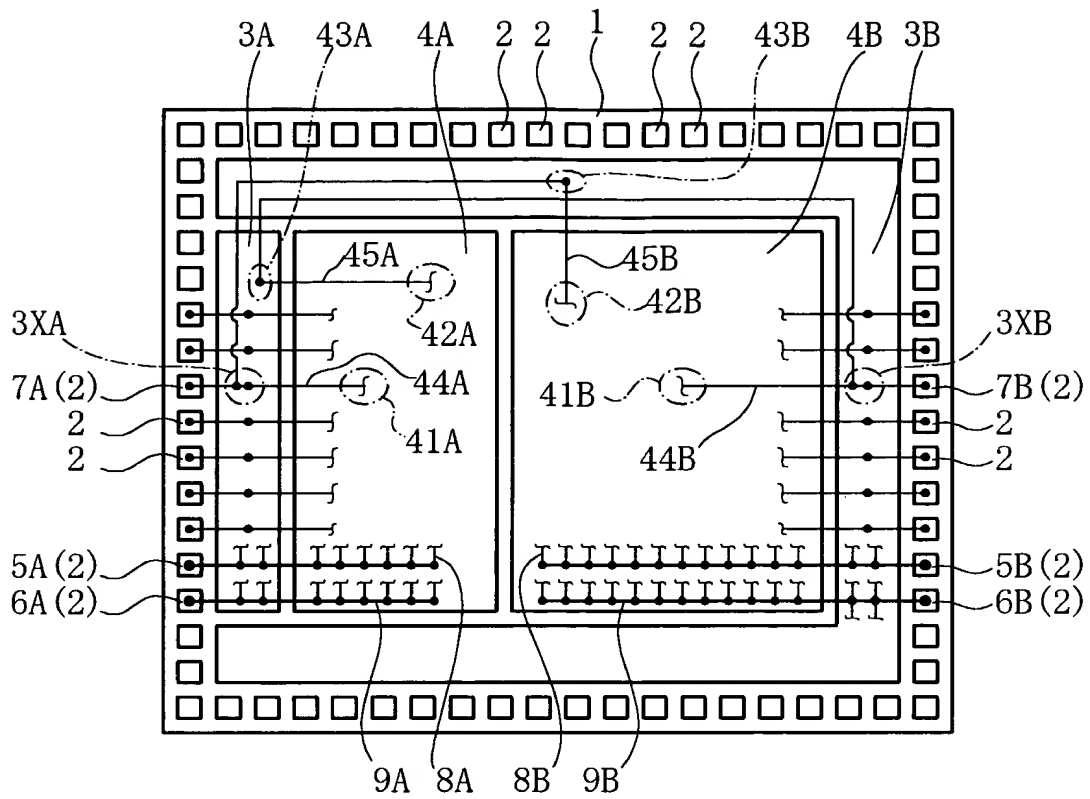


Fig. 7

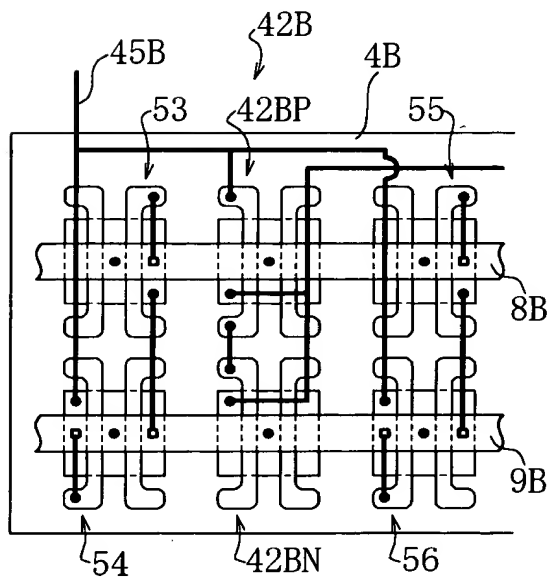


Fig. 8A

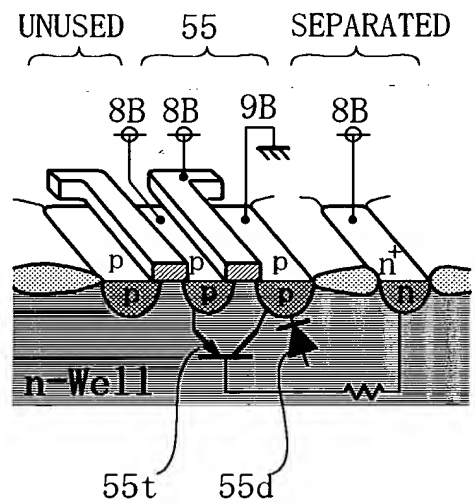


Fig. 8B

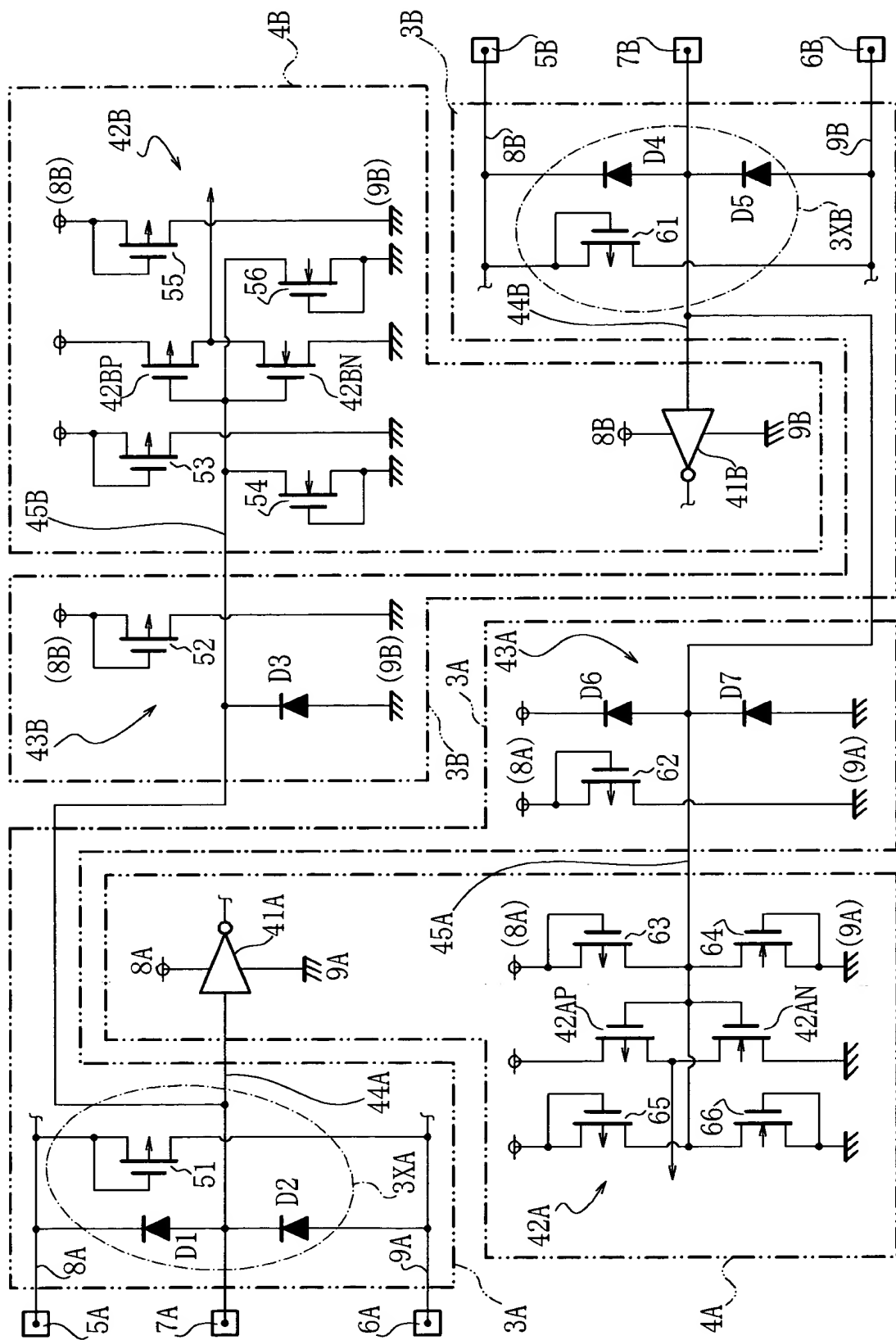


Fig. 9



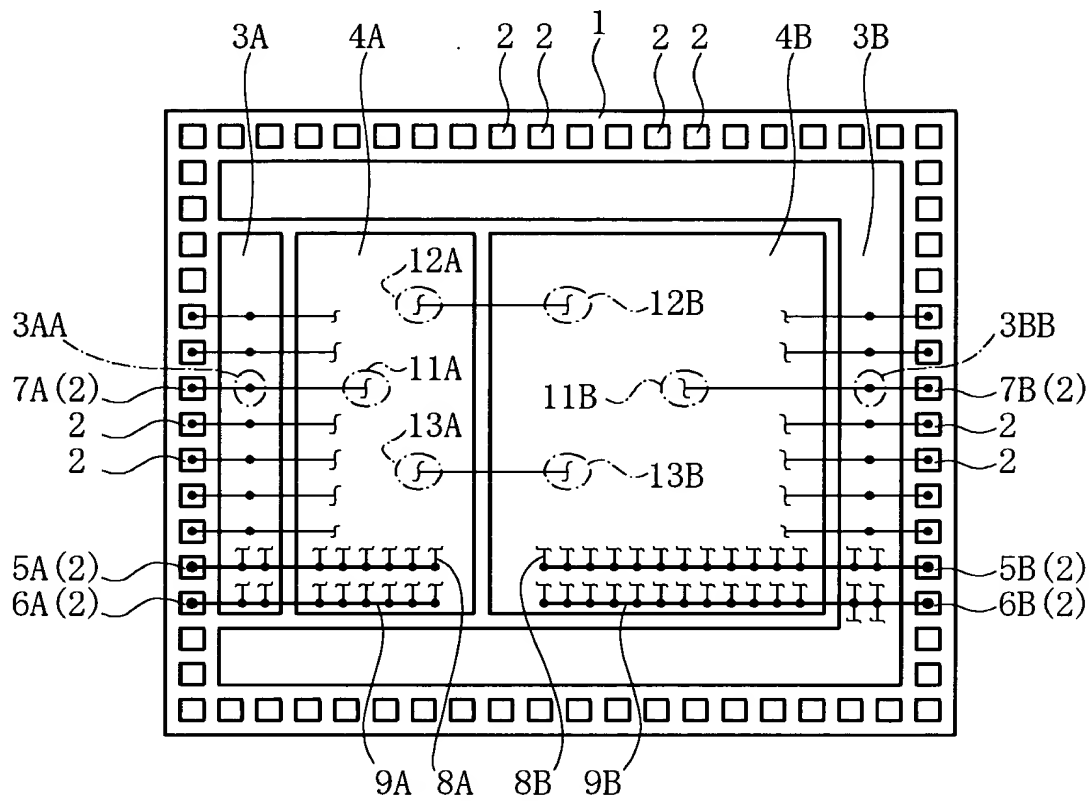


Fig. 10A

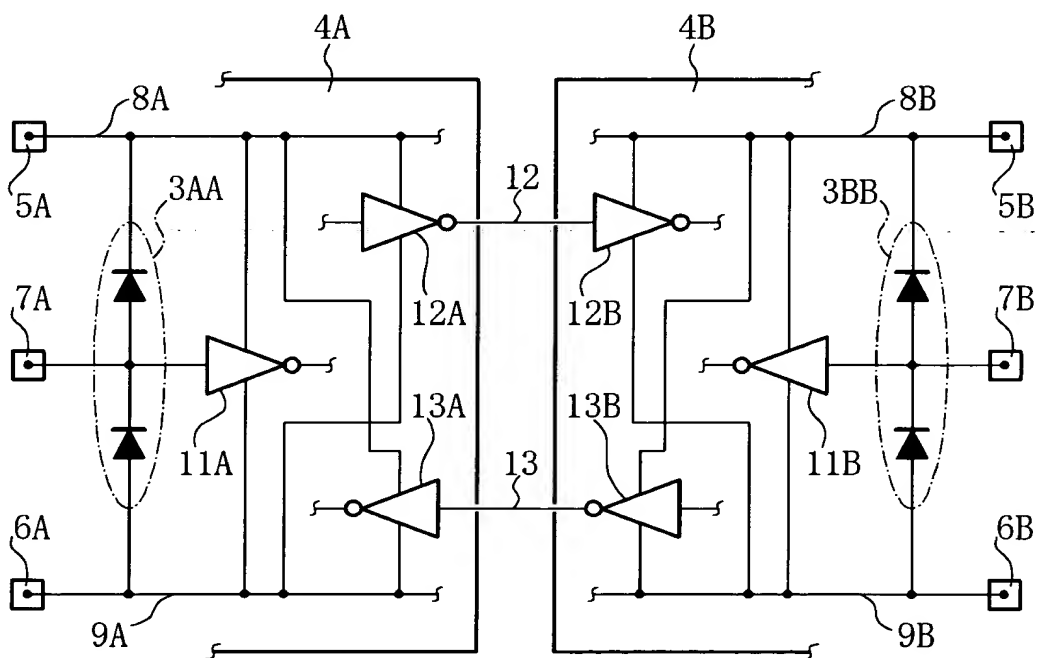


Fig. 10B

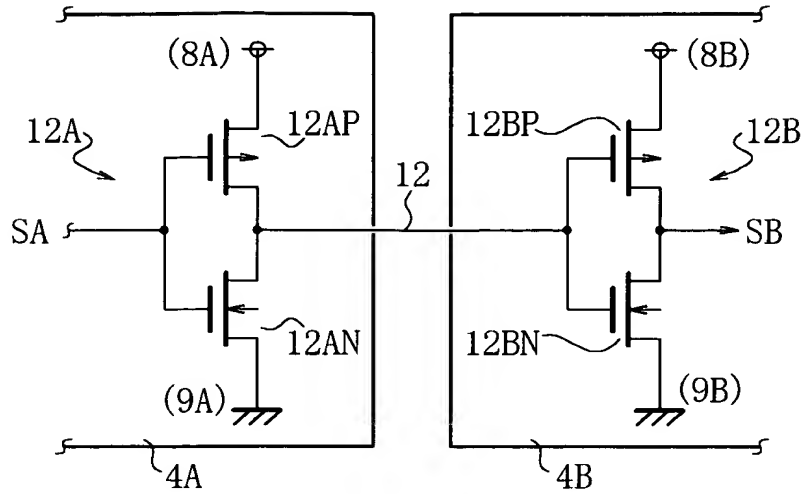


Fig. 11A

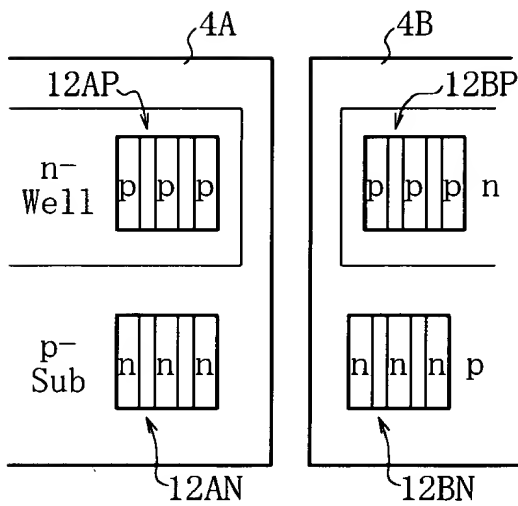


Fig. 11B

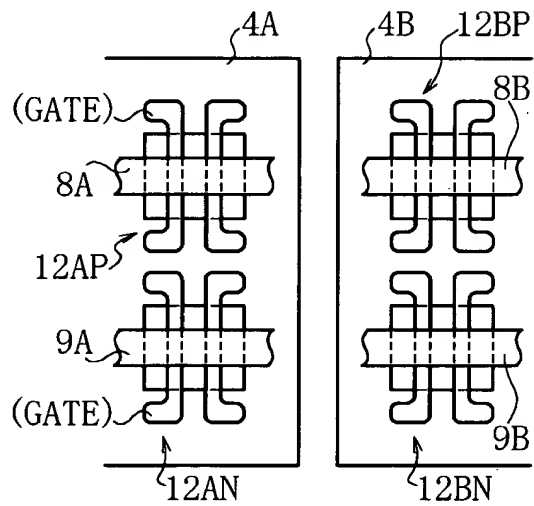


Fig. 11C

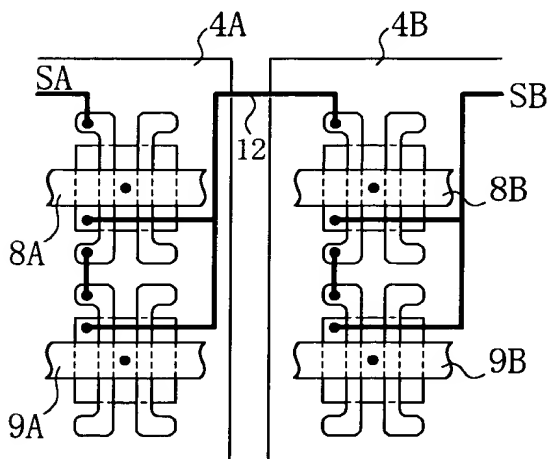


Fig. 11D

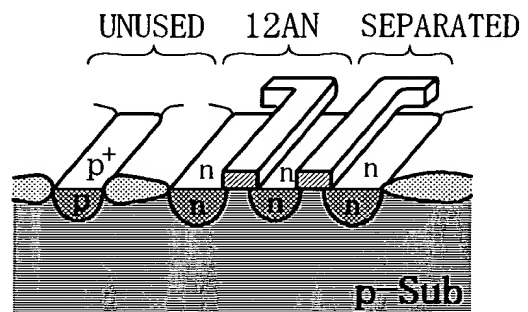


Fig. 11E

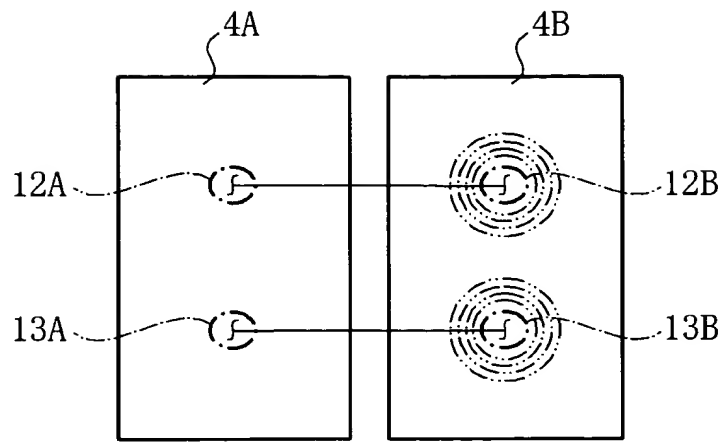


Fig. 12A

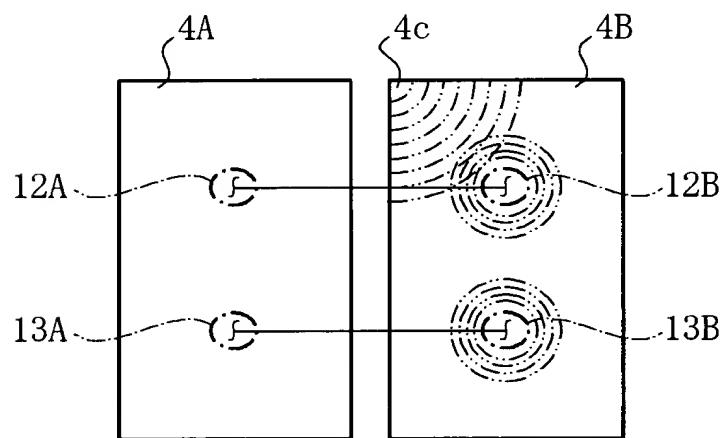


Fig. 12B

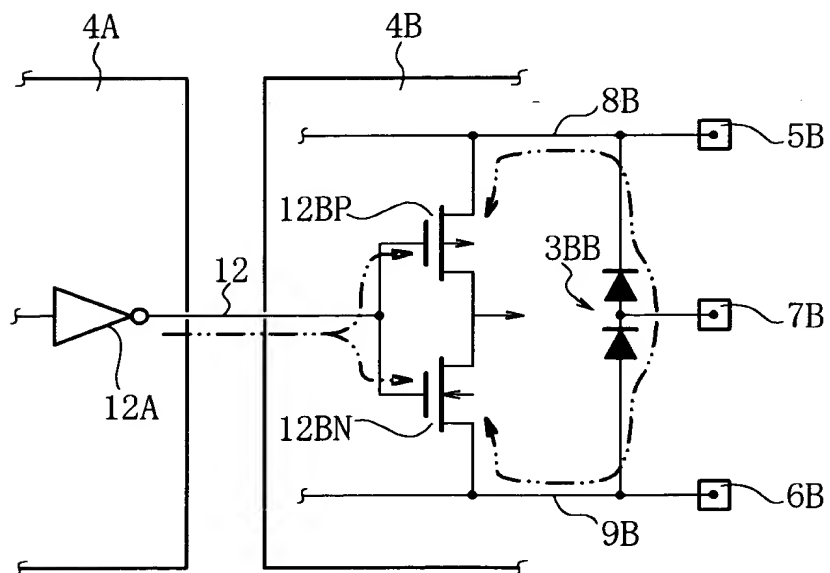


Fig. 12C